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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
SANDVIK, BENJAMIN P	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 04/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/759,183	MATSUO, MIE	
	Examiner	Art Unit	
	Ben P. Sandvik	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) 1-20 is/are rejected.

7)☐ Claim(s) 20 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 20 is objected to because of the following informalities: the lines "wherein a through plug is formed ... the semiconductor substrate" are redundant from claim 3. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3, 4, 6, 7, 9, 13, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mashino et al (U.S. PG Pub #20020190375), hereafter known as Mashino, in view of Mayazumi (U.S. PG Pub #20020079525).

With respect to **claim 1, 4, 7, and 13**, Mashino teaches a semiconductor substrate (Fig. 10, 201), a plug comprised of copper (Paragraph 146) and an insulation layer of silicon oxide (Fig. 10, 209 and Paragraph 83) that is disposed through an insulation film and semiconductor substrate (Fig. 10, 217), and a pattern portion comprised of copper that is not in contact with and partly surrounding the plug (Fig. 10, 205b and Paragraph 117), but does not teach a plurality of diffusion layer patterns formed on the substrate, an insulation film

formed between the plural diffusion layer patterns, and that the plug is partly surrounded by an insulation film formed on the substrate.

Mayazumi teaches a plurality of diffusion layer patterns formed on the substrate (Fig. 7, 10b), an insulation film formed between the plural diffusion layer patterns on the substrate (Fig. 7, 15), a plug (Fig. 7, 8a and 12d) formed to be partly surrounded by the insulation film (Fig. 7, 9) without being in contact with the plural diffusion layer patterns. It would have been obvious to one of ordinary skill in the art at the time the invention was made to fabricate the plurality of diffusion layer patterns and insulation film formed between the plural diffusion layer patterns in Mayazumi on the substrate of Mashino in order to give the device the capability to realize transistor circuits.

With respect to **claim 3, 6, 9, and 15**, Mashino teaches a plurality of semiconductor chips (Fig. 11), a semiconductor substrate (Fig. 10, 201), a plug comprised of copper (Paragraph 146) and an insulation layer of silicon oxide (Fig. 10, 209 and Paragraph 83) that is disposed through an insulation film and semiconductor substrate (Fig. 10, 217), a connecting member electrically connecting the through plugs of at least two semiconductor chip (Fig. 11, 210), and a pattern portion comprised of copper that is not in contact with and partly surrounding the plug (Fig. 10, 205b and Paragraph 117), but does not teach a plurality of diffusion layer patterns formed on the substrate, an insulation film

formed between the plural diffusion layer patterns, and that the plug is partly surrounded by an insulation film formed on the substrate.

Mayazumi teaches a plurality of diffusion layer patterns formed on the substrate (Fig. 7, 10b), an insulation film formed between the plural diffusion layer patterns on the substrate (Fig. 7, 15), a plug (Fig. 7, 8a and 12d) formed to be partly surrounded by the insulation film (Fig. 7, 9) without being in contact with the plural diffusion layer patterns. It would have been obvious to one of ordinary skill in the art at the time the invention was made to fabricate the plurality of diffusion layer patterns and insulation film formed between the plural diffusion layer patterns in Mayazumi on the substrate of Mashino in order to give the device the capability to realize transistor circuits.

Claims 2, 5, 8, 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mashino, in view of Mikawa et al (U.S. PG Pub #20020115226).

With respect to **claim 2, 5, 8, and 14**, Mashino teaches a semiconductor substrate (Fig. 10, 201), a plug comprised of copper (Paragraph 146) and an insulation layer of silicon oxide (Fig. 10, 209 and Paragraph 83) that is disposed through an insulation film and semiconductor substrate (Fig. 10, 217), and a pattern portion comprised of copper that is not in contact with and partly surrounding the plug (Fig. 10, 205b and Paragraph 117), but does not teach a plurality of diffusion layer patterns formed on the substrate, an insulation film

formed between the plural diffusion layer patterns, and that the plug is partly surrounded by an insulation film formed on the substrate.

Mikawa teaches a plurality of diffusion layer patterns formed on the substrate (Fig. 1, 11a), an insulation film formed between the plural diffusion layer patterns on the substrate (Fig. 1, 12), a plug (Fig. 1, 14) formed to be partly surrounded by the by the diffusion layer pattern without being in contact with the plural diffusion layer patterns. It would have been obvious to one of ordinary skill in the art at the time the invention was made to fabricate the plurality of diffusion layer patterns and insulation film formed between the plural diffusion layer patterns in Mikawa on the substrate of Mashino in order to give the device the capability to realize transistor circuits.

Claims 10 and12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mashino and Mayazumi, further in view of Mayashita et al (U.S. PG Pub #2001045605).

With respect to **claim 10**, Mashino and Mayazumi teach all of the limitations of claim 1, but do not teach that the plural diffusion layer patterns have a metal silicide layer. Mayashita teaches a diffusion layer pattern comprising a metal silicide layer (Paragraph 4). It would have been obvious to one of ordinary skill in the art at the time the invention was made to dispose a metal silicide layer as taught by Mayashita on the diffusion layer patterns of Mashino and Mayazumi in order to decrease the parasitic resistance of the device.

With respect to **claim 12**, Mashino and Mayazumi teach all of the limitations of claim 3, but do not teach that the plural diffusion layer patterns have a metal silicide layer. Mayashita teaches a diffusion layer pattern comprising a metal silicide layer (Paragraph 4). It would have been obvious to one of ordinary skill in the art at the time the invention was made to dispose a metal silicide layer as taught by Mayashita on the diffusion layer patterns of Mashino and Mayazumi in order to decrease the parasitic resistance of the device.

Claim 11 rejected under 35 U.S.C. 103(a) as being unpatentable over Mashino and Mikawa, further in view of Mayashita.

With respect to **claim 11**, Mashino and Mikawa teach all of the limitations of claim 2, but do not teach that the plural diffusion layer patterns have a metal silicide layer. Mayashita teaches a diffusion layer pattern comprising a metal silicide layer (Paragraph 4). It would have been obvious to one of ordinary skill in the art at the time the invention was made to dispose a metal silicide layer as taught by Mayashita on the diffusion layer patterns of Mashino and Mayazumi in order to decrease the parasitic resistance of the device.

Claims 16, and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mashino and Mayazumi, further in view of Koga (U.S. PG Pub #20020079492).

With respect to **claim 16**, Mashino and Mayazumi teach all of the limitations of claim 1, but do not teach the diameter of the through plug being

larger than an interval between adjacent diffusion layer patterns. Koga teaches a plug (Fig. 3d, 113) with a diameter that is larger than an interval between diffusion layer patterns (Fig. 3d, 108). It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the plug in Mashino and Mayazumi with a diameter that is larger than an interval between diffusion layer patterns as taught in Koga in order to create a larger contact area to receive a connection from an outside device.

With respect to **claim 18**, Mashino and Mayazumi teach all of the limitations of claim 3, but do not teach the diameter of the through plug being larger than an interval between adjacent diffusion layer patterns. Koga teaches a plug (Fig. 3d, 113) with a diameter that is larger than an interval between diffusion layer patterns (Fig. 3d, 108). It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the plug in Mashino and Mayazumi with a diameter that is larger than an interval between diffusion layer patterns as taught in Koga in order to create a larger contact area to receive a connection from an outside device.

With respect to **claim 19**, Mashino and Mayazumi teach all of the limitations of claim 1, but do not teach the diameter of the through plug being larger than a size of the diffusion layer patterns. Koga teaches a plug (Fig. 3d, 113) with a diameter that is larger than a size of the diffusion layer patterns (Fig. 3d, 108). It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the plug in Mashino and Mayazumi with a

diameter that is larger than a size of the diffusion layer patterns as taught in Koga in order to create a larger contact area to receive a connection from an outside device.

With respect to **claim 20**, Mashino and Mayazumi teach all of the limitations of claim 3, but do not teach the diameter of the through plug being larger than a size of the diffusion layer patterns. Koga teaches a plug (Fig. 3d, 113) with a diameter that is larger than a size of the diffusion layer patterns (Fig. 3d, 108). It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the plug in Mashino and Mayazumi with a diameter that is larger than a size of the diffusion layer patterns as taught in Koga in order to create a larger contact area to receive a connection from an outside device.

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mashino and Mikawa, further in view of Koga.

With respect to **claim 17**, Mashino and Mikawa teach all of the limitations of claim 2, but do not teach the diameter of the through plug being larger than an interval between adjacent diffusion layer patterns. Koga teaches a plug (Fig. 3d, 113) with a diameter that is larger than an interval between diffusion layer patterns (Fig. 3d, 108). It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the plug in Mashino and Mayazumi with a diameter that is larger than an interval between diffusion layer

patterns as taught in Koga in order to create a larger contact area to receive a connection from an outside device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ben P. Sandvik whose telephone number is (571) 272-8446. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
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